REMARKS

OVERVIEW

Claims 1 through 4 and 8 are pending in this application. Claims 5, 6 and 7 have been cancelled. Claim 1 has been amended.

ISSUES UNDER 35 U.S.C. § 102

Claims 1-2, and 6-8 have been rejected under 35 U.S.C. § 102(b) as being anticipated by JP 9-63805 to Yamada et al. et al. It is respectfully submitted that Yamada et al. cannot anticipate. In amended claim 1, the opposite parallel symmetric surfaces are now called the --top-- and --bottom-- surfaces instead of the "first" and "second" surfaces to clarify that there are two separate surfaces of the substrate that are opposite and symmetrical about the central longitudinal plane of the substrate. It is respectfully submitted that in Yamada et al., all resistive layers are formed on the same surface and not on two separate surfaces. Therefore, this rejection should be withdrawn as to claim 1.

In addition, claim 1 now requires "first and second terminals for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being substantially symmetrical about the central longitudinal plane." It is respectfully submitted that Yamada et al. does not disclose this limitation either.

Further, Yamada et al. has as its object, the goal of improving precision of a low-value resistor by separate adjustment of four isolated segments of the resistive layer. After adjustment, all of the segments are connected in parallel by resistor terminals. Thus, Yamada et al. is directed towards a different type of problem than the claimed invention. In particular, Yamada et al. is not directed towards improved pulsed power tolerance in a chip resistor, but rather towards a precision resistor. This splitting of the resistive layer into smaller segments is structurally

different because the resistive layers are still formed on the same surface of the chip resistor substrate, as opposed to "opposite parallel symmetrical top and bottom surfaces." Thus, Yamada et al. would not eliminate thermal bending because the chip remains asymmetrical about the central longitudinal plane. Yamada et al. does not increase the surface for a resistive layer by having two surfaces of the resistor. Claim 1 also now requires the limitation previously found in now cancelled claim 5 "wherein an area of the first resistive layer is substantially equal to an area of the second resistive layer such that the chip resistor with both resistive layers tolerates higher and instantaneous pulsed power than either layer could provide separately and individually." Yamada et al. does not disclose this limitation either.

Therefore, it is respectfully submitted that this rejection to claim 1 is now improper and should be withdrawn. As claims 2 and 8 depend from claim 1, these rejections should also be withdrawn. As claims 6 and 7 have been cancelled, these rejections are moot.

Further, with respect to claim 8, the Examiner indicates that Yamada et al. discloses a first resistive layer and second resistive layer symmetrical about the central longitudinal plane (Office Action, page 3). The Applicant respectfully disagrees. In particular, claim 8 is dependent from claim 1 that requires that the substrate have "opposite parallel symmetrical top and bottom surfaces, and a central longitudinal plane of symmetry." Claim 1 also requires "separate and spaced first and second resistive layers on the top and bottom surfaces." Thus, the first resistive layer and the second resistive layer are parallel to the central longitudinal plane. Yamada et al. does not disclose resistive layers symmetric about any plane that is parallel to them. Therefore, there is an independent basis for removing this rejection to claim 8.

Claims 1 and 5-8 have been rejected under 35 U.S.C. § 102(e) as being anticipated by

U. S. Patent No. 6,404,324 to Witt et al. et al. Claims 5-7 have been cancelled, thereby mooting these rejections. Previous claim 5, however, has been incorporated into amended claim 1. It is respectfully submitted that these rejections should also be withdrawn.

Witt et al. discloses a two-sided flat resistor. Witt et al. discloses offsetting of substrate bending to eliminate catastrophic failure of a resistive layer. Witt et al. does not disclose a resistor suitable for direct loading to a pick-and-place machine for a bulk case without concern for a top-bottom orientation, as Witt et al. is not directed towards a chip resistor that is symmetrical with respect to its top-bottom orientation.

For example, the termination shown in Witt et al. has four wires for through-hole mounting connected to top and bottom resistive layers. The terminals would be inherently non-symmetric about the central longitudinal plane. Claim 1 has been amended to explicitly require "first and second terminals for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being substantially symmetrical about the central longitudinal plane." This limitation is not disclosed in Witt et al., and therefore this rejection to claim 1 should be removed.

It is further noted that Witt et al. is directed towards solving a different type of problem than that which the present invention is directed to. Witt et al. is directed towards a high-power resistor that is expected to tolerate long-duration (in the range of seconds) electrical pulses (see column 6, line 40). The present invention is directed towards surface mounted chip resistors, and the doubling of resistor pulse load capability would be relevant only to short-time pulses.

Further, because, claim 1 requires, "first and second terminals for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being substantially symmetrical about the central longitudinal plane", the chip resistor of the present

invention is "symmetrical to allow for direct loading to a pick-and-place machine without concern for top-bottom orientation." This functional advantage or structure that would provide this functional advantage is simply not disclosed in Witt et al. Witt et al. is not directed towards a surface mount resistor. Furthermore, Witt et al. would not be appropriate for "direct loading to a pick-and-place machine without concern for top-bottom orientation." Therefore, because Witt et al. is directed towards solving a different problem in a different manner, and due to the claimed structural differences and resulting functional advantages, this rejection to claim 1 is now inappropriate and should now be withdrawn. As claims 2-4 and 8 depend from claim 1, these rejections should also be withdrawn.

ISSUES UNDER 35 U.S.C. § 103

Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Witt et al. in view of U. S. Patent No. 5,543,775 to Huck. Huck discloses using thin film resistive layers. The Examiner rejects claim 4 under 35 U.S.C. § 103(a) over Witt et al. in view of U.S. Patent No. 4,064,477 to Thompson. Thompson discloses using foil resistive layers. These rejections should be withdrawn. Neither Huck nor Thompson discloses the limitations of claim 1 that are not disclosed by Witt et al. In particular, neither reference, for example, provides for "first and second terminals for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being substantially symmetrical about the central longitudinal plane" such that a chip resistor is formed "being symmetrical to allow for direct loading to a pick-and-place machine without concern for top-bottom orientation." Therefore, as claims 3 and 4 depend from claim 1, these rejections should also be withdrawn.

CONCLUSION

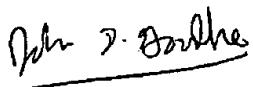
The Applicant respectfully submits that all present claims are in proper form for

immediate allowance. No fees or extensions of time are believed to be due in connection with this amendment; however, consider this a request for any extension inadvertently omitted, and charge any additional fees to Deposit Account No. 26-0084.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Reconsideration and allowance is respectfully requested.

Respectfully submitted,



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Application No. **10/002,868**

AMENDMENT — VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

1. (Amended)

1. A chip resistor being symmetrical to allow for direct loading to a pick-and-place machine without concern for top-bottom orientation, comprising:

a substrate having opposite parallel symmetrical ~~first~~ top and ~~second~~ bottom surfaces, and a central longitudinal plane of symmetry;

separate and spaced first and second resistive layers on the ~~first~~ top and ~~second~~ bottom surfaces, respectively, electrically connected in parallel to each other; and

the ~~first~~ top and ~~second~~ bottom surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof~~.~~;

wherein an area of the first resistive layer is substantially equal to an area of the second resistive layer such that the chip resistor with both resistive layers tolerates higher instantaneous pulsed power than either layer could provide separately and individually; and

first and second terminals for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being substantially symmetrical about the central longitudinal plane.